REMARKS

Examiner T. Phan is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 14, and 26 have been amended and Claims 2 and 15 have been canceled.

The drawing Fig. 5 has been corrected in red to show the transistors 46c-46n, but to remove the additional element 52 added in response to the previous office action. It is believed that this element 52 is the new matter referred to by the Examiner in paragraph 3 of the instant office action. The Specification has been amended to remove reference to element 52.

Reconsideration of the rejection of Claims 1 and 4 under 35 U.S.C. 112, first paragraph and the related objection to the drawings is requested in view of amended Claims 1 and 4. The "end user" has been deleted from Claims 1 and 4. The "end user" has been replaced with "in normal operation" (see the first full paragraph of page 9). It is believed that this amendment overcomes both the rejection of the claims and the objection to the drawings.

Reconsideration of the rejection of Claims 1-27 under 35 U.S.C. 112, first paragraph is requested in view of the amendments to the Specification and corrected Fig. 5. Fig. 5 shows the circuitry internal to the EPROM used to generate the erase voltages for normal and margin erasing. See page 5 where the objects of the invention include a Flash EPROM device having an internally generated marginal erase voltage and page 6, second paragraph, where it is stated that the marginal erase circuitry of the EPROM comprises the elements depicted in Fig. 5. It is also stated that the erase voltage is applied at the charge pump, as shown by VE in Fig. 5. The top of page 10 discusses the point of application of the erase voltage VE. It will be understood by those skilled in the art that the erase voltage is applied to erase the EPROM memory cell. An internally generated erase voltage will be understood to be applied to the EPROM memory cell within which it is generated.

All Claims are believed to be in condition for Allowance, and that is so requested. It is requested that should the Examiner not find that the claims are now allowable, that the Examiner enter the amendment for purposes of Appeal.

Reconsideration of the rejection under 35 U.S.C. 102(b) of Claims 1-27 as being anticipated by Sansbury is requested in view of amended Claims 1, 14, and 26 and in accordance with the following remarks.

Claim 1 has been amended to incorporate dependent Claim 2 claiming that the margin erase voltage is reduced over the normal erase voltage. Claim 14 has been amended to incorporate dependent Claim 15 claiming that the margin erase voltage is reduced over the normal erase voltage by a plurality of series connected voltage dropping devices and that the margin erase voltage is reduced by n times the voltage of one of the voltage dropping devices where n is the number of voltage dropping devices connected in series. (See page 10 of the Specification). Claim 26 has been amended to incorporate the details of the reduction of the margin erase voltage over the normal erase voltage as claimed in amended Claims 1 and 14.

It is agreed that Sansbury discloses margin testing of a memory cell. However, this reference uses the threshold erase voltage during margin test procedure rather than a reduced voltage (col. 15, lines 29-41). The amended Claims claim a reduced margin erase voltage. Thus, Applicants' invention is different from Sansbury in the value of the margin erase voltage.

Reconsideration of the rejection under 35 U.S.C. 102(b) of Claims 1-27 as being anticipated by Sansbury is requested in view of amended Claims 1, 14, and 26 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1-27 as being unpatentable over Kim in view of Nomiya et al is requested in view of Amended Claims 1, 14, and 26 and in accordance with the following remarks.

Applicants' invention comprises a functional circuit (core circuit) and a testing circuit. Kim discusses lowering the erase voltage output from a charge pump in a functional circuit (cols 1-2). Applicants' invention provides a testing method to confirm the endurance of a Flash device by the testing circuit. Kim does not mention testing at all and so has nothing to do with the device, method, and detailed claims of Applicants' invention. Nomiya et al discloses a protective diode to prevent loss of memory due to noise (col. 7, lines 14-32). Applicants' invention has to do with erase voltage generation. Thus, Noyima et al has nothing to do with Applicants' invention. The two references individually and in combination fail to teach or suggest Applicants' invention wherein an internally generated margin erase voltage is lower than a normal erase voltage.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 1-27 as being unpatentable over Kim in view of Nomiya et al is requested in view of Amended Claims 1, 14, and 26 and in accordance with the remarks above.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner Phan not find that the Claims are now Allowable that the Examiner call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

Rosemary L. S. Pike. Reg # 39,332

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please replace the third paragraph of page 8 with the following:

Refer now to Fig. 5, schematically depicting the method of the present invention. A Flash EPROM cell [52] is to be erased. The cathode of a protective diode 38 is connected to a charge pump circuitry 36. The anode of the protective diode 38 is connected to one (or more) diode-connected NMOS transistor(s) 40, for example. A diode-connected NMOS transistor is one where the drain and gate are connected. When conducting, the voltage drop across each diode-connected NMOS transistor will be equal to the transistor threshold voltage (V_t).

Please replace the first full paragraph of page 9 with the following:

The function of the margin erase circuit of the present invention is now described. During normal operation of the Flash EPROM cell [52], the bypass switch 50 is opened. The voltage, V_E, regulated by this regulator will be the normal erase voltage (V_{NE}), which is the sum of the voltage drops across transistors 46a-46n and 40 and the breakdown voltage (V_{bd}) of the protective diode 38. Since the voltage drop across each transistor 46a-46n and 40 is equal to V_t (threshold voltage of NMOS transistor), the normal erase voltage observed at the cathode of the protective diode 38 is given by:

$$V_{NE} = V_{bd} + V_t + n*V_t .$$

During testing of the Flash EPROM cell [52], the bypass switch 50 is closed thereby bypassing transistors 46a-46n. This reduces the voltage observed at the cathode of the protective diode 38 by $n*V_t$. Thus, the margin erase voltage is given by:

$$V_{ME} = V_{bd} + V_t.$$

IN THE CLAIMS

Please amend the Claims as follows.

1. (TWICE AMENDED) A method of margin erasing memory cells in a testing procedure of a flash EPROM memory in an integrated circuit wherein said margin erasing uses charge pump circuitry to develop both a normal erase voltage used [by an end user] in normal operation and a margin erase voltage used in said testing procedure wherein said margin erase voltage applied to said memory cells during said margin erasing is reduced over said normal erase voltage.

Please cancel Claim 2.

14. (TWICE AMENDED) A method of margin erasing memory cells in a testing procedure of a flash EPROM memory in an integrated circuit wherein said margin erasing uses an internal charge pump circuit to develop both a normal erase voltage used [by an end user] in normal operation and a margin erase voltage used in said testing procedure and wherein said margin erase voltage applied to said memory cells during

said margin erasing is reduced over said normal erase voltage by bypassing series connected voltage dropping components wherein said voltage is reduced by n times a voltage of one of said voltage dropping components where n is the number of voltage dropping components connected in said series.

Please cancel Claim 15.

26. (TWICE AMENDED) A flash EPROM memory device comprising:

a charge pump circuit;

a protective diode having a cathode and an anode wherein said cathode of said protective diode is connected to said charge pump circuit;

a plurality of series connected voltage dropping devices wherein a drain of a first of said plurality of series connected voltage dropping devices is connected to said anode of said protective diode;

a bias current source connected to a source of said last of said plurality of series connected voltage dropping devices; and

a bypass switch to bypass one or more of said series connected voltage dropping devices wherein during normal operation of said flash EPROM memory device, said plurality of series connected voltage dropping devices is not bypassed to provide a normal erase voltage and wherein during margin erasing, said plurality of series connected voltage dropping devices is bypassed thereby providing a margin erase voltage that is lower than said normal erase voltage.